	Type	L #	Hits	Search Text	DBs
1	BRS	L1	19	("20020034646"|"20030020060"|"20040043208"|"20050053773"|"20050062033"|"20060043410"|"20060060924"|"5201681"|"5361015"|"5422302"|"5458755"|"5726464"|"5874047"|"6309945"|"6448155"|"6468923"|"6613676"|"6936854"|"6972146").PN.	US-PGPUB; USPAT
2	BRS	L2	89766	field near8 effect near8 transistor	US-PGPUB; USPAT
3	BRS	L3	79785	2 and (pore or hole or well or channel)	US-PGPUB; USPAT
4	BRS	L4	6947	3 and (pore or hole or well or channel) with silicon near8 oxide	US-PGPUB; USPAT
5	BRS	L5	32822	3 and (pore or hole or well or channel) with (insulating or semiconductor)	US-PGPUB; USPAT
6	BRS	L6	57	4 and (chemical or biochemical) near8 (sensor or detector)	US-PGPUB; USPAT
7	BRS	L7	1	6 and pillar	US-PGPUB; USPAT
8	BRS	L8	15	6 and antibod$9	US-PGPUB; USPAT
9	BRS	L9	12	("5063164" | "5111221" | "5393401" | "5618493").PN. OR ("5874047").URPN.	US-PGPUB; USPAT; USOCR

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 NEWS  8  MAY 30   IPC 8 Rolled-up Core codes added to CA/CAplus and
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 NEWS  9  MAY 30   The F-Term thesaurus is now available in CA/CAplus
 NEWS 10  JUN 02   The first reclassification of IPC codes now complete in
                   INPADOC
 NEWS 11  JUN 26   TULSA/TULSA2 reloaded and enhanced with new search and
                   and display fields
 NEWS 12  JUN 28   Price changes in full-text patent databases EPFULL and PCTFULL
 NEWS 13  JUl 11   CHEMSAFE reloaded and enhanced
 NEWS 14  JUl 14   FSTA enhanced with Japanese patents
 NEWS 15  JUl 19   Coverage of Research Disclosure reinstated in DWPI

 NEWS EXPRESS  JUNE 30 CURRENT WINDOWS VERSION IS V8.01b, CURRENT
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Compendex Compilation and Indexing (C) 2006


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=> s field effect transistor
L1       81013 FIELD EFFECT TRANSISTOR

=> s l1 and (source or drain) (8a) region?
L2        4582 L1 AND (SOURCE OR DRAIN) (8A) REGION?

=> s l2 and (porous or pores or holes) (s) film
L3          31 L2 AND (POROUS OR PORES OR HOLES) (S) FILM

=> s l3 and biosensor
L4           0 L3 AND BIOSENSOR

=> s l3 and (sensor or detector)
L5           0 L3 AND (SENSOR OR DETECTOR)

=> s l2 and (porous or pores or holes)
L6         201 L2 AND (POROUS OR PORES OR HOLES)

=> s l6 and immobiliz? (8a) antibod?
L7           0 L6 AND IMMOBILIZ? (8A) ANTIBOD?

=> s l6 and antibod?
L8           0 L6 AND ANTIBOD?

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L9          179 DUPLICATE REMOVE L6 (22 DUPLICATES REMOVED)

=> s l9 and mean pore density
L10          0 L9 AND MEAN PORE DENSITY

=> s l9 and silicon ?oxide
L11         11 L9 AND SILICON ?OXIDE

=> display l11 1-11 ibib abs

L11  ANSWER 1 OF 11  CAPLUS  COPYRIGHT 2006 ACS on STN
ACCESSION NUMBER:        2006:319309  CAPLUS
DOCUMENT NUMBER:         144:361535
TITLE:                   Semiconductor device and manufacturing method thereof
INVENTOR(S):             Inaba, Satoshi
PATENT ASSIGNEE(S):      Kabushiki Kaisha Toshiba, Japan
SOURCE:                  U.S. Pat. Appl. Publ., 27 pp.
                         CODEN: USXXCO
DOCUMENT TYPE:           Patent
LANGUAGE:                English
FAMILY ACC. NUM. COUNT:  1
PATENT INFORMATION:

     PATENT NO.          KIND   DATE        APPLICATION NO.        DATE
```

US 2006073647	A1	20060406	US 2004-5477	20041207
JP 2006100731	A2	20060413	JP 2004-287702	20040930
CN 1763950	A	20060426	CN 2005-10108757	20050930

PRIORITY APPLN. INFO.: JP 2004-287702 A 20040930

AB A semiconductor device comprising a multi Fin-FET structure capable of suppressing short channel effects, controlling a threshold voltage, driving a high current, and operating in a high-speed comprises a source region and a drain region disposed on a semiconductor substrate, a plurality of fins interconnecting the source region and drain region , a first gate electrode disposed on the semiconductor substrate and to one side face of each fin, a second gate electrode disposed on the semiconductor substrate and to the other side face of the fin to face the first gate electrode, and separated from the first gate electrode, a plurality of first pad electrodes connected to resp. first gate electrode, a first wiring interconnecting the plurality of first pad electrodes, a plurality of second pad electrodes connected to resp. second gate electrode, and a second wiring interconnecting the plurality of second pad electrodes.

L11 ANSWER 2 OF 11 CAPLUS COPYRIGHT 2006 ACS on STN
ACCESSION NUMBER: 2005:220220 CAPLUS
DOCUMENT NUMBER: 142:307954
TITLE: Structure and method for silicided metal gate transistors
INVENTOR(S): Doris, Bruce B.; Zhu, Huilong
PATENT ASSIGNEE(S): International Business Machines Corporation, USA
SOURCE: U.S. Pat. Appl. Publ., 19 pp.
CODEN: USXXCO
DOCUMENT TYPE: Patent
LANGUAGE: English
FAMILY ACC. NUM. COUNT: 1
PATENT INFORMATION:

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
US 2005055494	A1	20050310	US 2003-605130	20030910
US 6908850	B2	20050621		
CN 1627486	A	20050615	CN 2004-10076817	20040907

PRIORITY APPLN. INFO.: US 2003-605130 A 20030910

AB An efficient and cost-effective method for fabricating metal gates of transistors is claimed. A structure and method are provided for fabricating a field effect transistor (FET) having a metal gate structure. A metal gate structure is formed in an opening within a dielec. region formerly occupied by a sacrificial gate. The metal gate structure includes a 1st layer contacting a gate dielec. formed over a semiconductor region of a substrate. The 1st layer includes a material selected from the group consisting of metals and metal compds. The gate further includes a silicide formed over the 1st layer. The FET further includes a source region and a drain region formed on opposite sides of the gate, the source and drain regions being silicided after the 1st layer of the gate is formed.

REFERENCE COUNT: 16 THERE ARE 16 CITED REFERENCES AVAILABLE FOR THIS RECORD. ALL CITATIONS AVAILABLE IN THE RE FORMAT

L11 ANSWER 3 OF 11 CAPLUS COPYRIGHT 2006 ACS on STN
ACCESSION NUMBER: 2004:219740 CAPLUS
DOCUMENT NUMBER: 140:244940
TITLE: Semiconductor device and method of manufacturing
INVENTOR(S): Kato, Toshikazu
PATENT ASSIGNEE(S): NEC Electronics Corporation, Japan
SOURCE: U.S. Pat. Appl. Publ., 16 pp.
CODEN: USXXCO

DOCUMENT TYPE: Patent
LANGUAGE: English
FAMILY ACC. NUM. COUNT: 1
PATENT INFORMATION:

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
US 2004051120	A1	20040318	US 2003-658720	20030909
US 6943411	B2	20050913		
JP 2004111634	A2	20040408	JP 2002-271807	20020918

PRIORITY APPLN. INFO.: JP 2002-271807 A 20020918

AB The present invention may include a semiconductor device having a low resistance embedded wiring layer formed on and extending over a semiconductor substrate, and a plurality of element regions formed over the embedded wiring layer. A semiconductor device can include a low resistance wiring layer formed in, and extending along a base material. A number of element regions are formed sep. from one another, each in contact with wiring layer. A circuit element can be formed in each element region. A metal is preferably used for wiring layer. In the above arrangement, metal-oxide-semiconductor type transistors can be provided in a Si-on-insulator substrate that can have different potentials applied to a source/drain region with respect to a channel region.

REFERENCE COUNT: 3 THERE ARE 3 CITED REFERENCES AVAILABLE FOR THIS RECORD. ALL CITATIONS AVAILABLE IN THE RE FORMAT

L11 ANSWER 4 OF 11 CAPLUS COPYRIGHT 2006 ACS on STN
ACCESSION NUMBER: 2004:147192 CAPLUS
DOCUMENT NUMBER: 141:63163
TITLE: Method for manufacture of power MOSFET
INVENTOR(S): Ni, Shenru
PATENT ASSIGNEE(S): Lisheng Semiconductors Co., Ltd., Peop. Rep. China
SOURCE: Faming Zhuanli Shenqing Gongkai Shuomingshu, 11 pp.
CODEN: CNXXEV
DOCUMENT TYPE: Patent
LANGUAGE: Chinese
FAMILY ACC. NUM. COUNT: 1
PATENT INFORMATION:

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
CN 1377066	A	20021030	CN 2001-110053	20010326

PRIORITY APPLN. INFO.: CN 2001-110053 20010326

AB The method comprises: (1) forming a gate dielec. layer on the heap crystal layer of a substrate, forming a patterned gate conductor layer on the gate dielec., and forming a lid having different etching rate than the gate dielec. (borophosphosilicate glass) on the gate conductive layer, (2) forming a well region in the area not covered by the gate lid, forming a source region in the well region, and ion implanting the heap crystal layer at 25-150 keV and 1 x 1015-3 x 1016 ions/cm2 for inhibition of oxidation of the crystal heap, (3) forming oxide spacer 2000-5000 Å thick at the side wall of the gate conductive layer (including polysilicon) by thermal oxidation, (4) forming a SiO2 buffer layer between the lid and the gate conductor, (5) forming a dielec. layer on the substrate and then forming contact windows by self-alignment technol., and (5) forming a window on the dielec. layer to expose the source electrode, forming a metal layer on the contact window and the dielec. layer, and elec. connecting the source electrode region.

L11 ANSWER 5 OF 11 CAPLUS COPYRIGHT 2006 ACS on STN
ACCESSION NUMBER: 2003:203089 CAPLUS
DOCUMENT NUMBER: 138:213763
TITLE: Vertical replacement-gate junction field-effect transistor

INVENTOR(S): Chaudhry, Samir; Layman, Paul Arthur; McMacken, John Russell; Thomson, Ross; Zhao, Jack Qingsheng
PATENT ASSIGNEE(S): Agere Systems Inc., USA
SOURCE: U.S. Pat. Appl. Publ., 18 pp.
CODEN: USXXCO
DOCUMENT TYPE: Patent
LANGUAGE: English
FAMILY ACC. NUM. COUNT: 1
PATENT INFORMATION:

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
US 2003047749	A1	20030313	US 2001-950384	20010910
US 6690040	B2	20040210		
GB 2383191	A1	20030618	GB 2002-20232	20020830
GB 2383191	B2	20060712		
TW 556289	B	20031001	TW 2002-91119882	20020830
JP 2003163280	A2	20030606	JP 2002-263479	20020910
US 2004110345	A1	20040610	US 2003-723547	20031126
US 7033877	B2	20060425		
US 2006166429	A1	20060727	US 2006-390015	20060327

PRIORITY APPLN. INFO.: US 2001-950384 A 20010910
US 2003-723547 A1 20031126

AB To provide further advances in the fabrication of JFETs having gate lengths precisely controlled through a deposited film thickness, an architecture is provided for fabricating vertical replacement gate JFET devices. Generally, an integrated circuit structure includes a semiconductor area with a major surface formed along a plane and a 1st source/drain doped region formed in the surface. A 2nd doped region forming a channel of different conductivity type than the 1st region is positioned over the 1st region. A 3rd doped region is formed over the 2nd doped region having an opposite conductivity type with respect to the 2nd doped region, and forming a source/drain region. A gate is formed over the channel to form a vertical JFET. In an associated method of manufacturing the semiconductor device, a 1st source/drain region is formed in a semiconductor layer. A field-effect transistor gate region, including a channel and a gate electrode, is formed over the 1st source/drain region. A 2nd source/drain region is then formed over the channel having the appropriate conductivity type.

L11 ANSWER 6 OF 11 CAPLUS COPYRIGHT 2006 ACS on STN
ACCESSION NUMBER: 2000:874181 CAPLUS
DOCUMENT NUMBER: 134:35969
TITLE: Method of depositing polysilicon, fabricating a field effect transistor, forming a contact to a substrate, and forming a capacitor
INVENTOR(S): Nuttall, Michael; Ping, Er-xuan; Hu, Yongjun Jeff
PATENT ASSIGNEE(S): Micron Technology, Inc., USA
SOURCE: U.S., 11 pp.
CODEN: USXXAM
DOCUMENT TYPE: Patent
LANGUAGE: English
FAMILY ACC. NUM. COUNT: 1
PATENT INFORMATION:

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
US 6159852	A	20001212	US 1998-23239	19980213
US 6509239	B1	20030121	US 1999-429236	19991028
US 2002048911	A1	20020425	US 2001-843116	20010424
US 6458699	B2	20021001		

US 2002155684	A1	20021024	US 2002-50426	20020115
US 6797558	B2	20040928		
US 2004224485	A1	20041111	US 2004-863046	20040607
US 7049231	B2	20060523		
US 2006019442	A1	20060126	US 2005-234328	20050923
US 2006019475	A1	20060126	US 2005-234334	20050923

PRIORITY APPLN. INFO.: US 1998-23239 A3 19980213
US 1999-429236 A3 19991028
US 2001-843116 A3 20010424
US 2002-50426 A3 20020115
US 2004-863046 A1 20040607

AB In a method of depositing polysilicon comprises providing a substrate within a CVD reactor, with the substrate having an exposed substantially crystalline region and an exposed substantially amorphous region. A gaseous precursor comprising Si is fed to the CVD reactor under conditions effective to selectively deposit polysilicon on the crystalline region and not the amorphous region. In another aspect a method of fabricating a field effect transistor on a substrate comprises forming a gate dielec. layer and a gate over semiconductive material. A gaseous precursor comprising Si is fed to the CVD reactor under conditions effective to substantially selectively deposit polysilicon on the source/drain regions and not on amorphous material, and forming elevated source/drains on the doped source/drain regions. In another aspect, a method of forming a contact to a substrate is disclosed. A contact opening is etched through amorphous insulating material over a node location ultimately comprising an outwardly exposed substantially crystalline surface. Within a CVD reactor, a gaseous precursor comprising Si is provided under conditions effective to selectively deposit polysilicon on the outwardly exposed crystalline node location surface and not on the insulating material.

REFERENCE COUNT: 20 THERE ARE 20 CITED REFERENCES AVAILABLE FOR THIS RECORD. ALL CITATIONS AVAILABLE IN THE RE FORMAT

L11 ANSWER 7 OF 11 CAPLUS COPYRIGHT 2006 ACS on STN
ACCESSION NUMBER: 1991:73594 CAPLUS
DOCUMENT NUMBER: 114:73594
TITLE: Field-effect transistor and its manufacture
INVENTOR(S): Okuda, Yasushi; Hirai, Takehiro
PATENT ASSIGNEE(S): Matsushita Electric Industrial Co., Ltd., Japan
SOURCE: Jpn. Kokai Tokkyo Koho, 4 pp.
CODEN: JKXXAF
DOCUMENT TYPE: Patent
LANGUAGE: Japanese
FAMILY ACC. NUM. COUNT: 1
PATENT INFORMATION:

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
JP 02203538	A2	19900813	JP 1989-24204	19890202

PRIORITY APPLN. INFO.: JP 1989-24204 19890202

AB A FET, which has a substrate, a device isolation region (A) on the substrate, and polycryst. Si source and drain formed in partially removed areas of A, is prepared by (a) forming A from Si oxide; (b) partial removal of A; (c) filling the resulting holes with polycryst. Si; (d) implanting n- or p-type impurity in the polycryst. Si; and (e) heating to diffuse the impurity into the substrate and form a doped area having different d. from the polycryst. Si. Thus, a FET prepared by using P and As as impurities showed no deterioration caused by the hot-carrier effect.

L11 ANSWER 8 OF 11 CAPLUS COPYRIGHT 2006 ACS on STN
ACCESSION NUMBER: 1989:17267 CAPLUS

DOCUMENT NUMBER: 110:17267
TITLE: A self-aligned field-effect transistor and method for its fabrication
INVENTOR(S): Griffin, Edward Lawrence; Sadler, Robert Allan; Geissberger, Arthur Eugene
PATENT ASSIGNEE(S): International Standard Electric Corp., USA
SOURCE: Eur. Pat. Appl., 5 pp.
CODEN: EPXXDW
DOCUMENT TYPE: Patent
LANGUAGE: English
FAMILY ACC. NUM. COUNT: 5
PATENT INFORMATION:

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
EP 275905	A2	19880727	EP 1988-100360	19880113
EP 275905	A3	19890830		
R: DE, FR, GB, IT, NL				
US 4956308	A	19900911	US 1987-4992	19870120
US 4965218	A	19901023	US 1988-235393	19880823

PRIORITY APPLN. INFO.:

US 1987-4992	A	19870120
US 1985-789523	B1	19851021
US 1987-2083	A2	19870112
US 1987-2084	B2	19870112
US 1987-113367	A2	19871021
US 1987-137309	A3	19871223

AB A method of making a self-aligned gate FET device comprises forming an active channel region on the surface of a semiconductor substrate; metalizing a gate region on the channel region relatively near a central portion thereof; forming a photoresist over the gate region to define a source and a drain region on either side of the gate region; opening holes in the photoresist on each side of the gate region with the photoresist extending a greater distance into the drain region than the source region; and doping the drain and source regions via the holes to provide asym. located source and drain regions as compared to the gate region, whereby the gate region has 1 side adjacent the source region and the other side separated a given distance from the drain region. Parasitic source resistance is reduced in the FET.

L11 ANSWER 9 OF 11 CAPLUS COPYRIGHT 2006 ACS on STN
ACCESSION NUMBER: 1987:649175 CAPLUS
DOCUMENT NUMBER: 107:249175
TITLE: Semiconductor chemical sensor
INVENTOR(S): Sakai, Tadashi; Uno, Shigeki; Shinho, Masaru; Furukawa, Kazuyoshi
PATENT ASSIGNEE(S): Toshiba Corp., Japan
SOURCE: Jpn. Kokai Tokkyo Koho, 8 pp.
CODEN: JKXXAF
DOCUMENT TYPE: Patent
LANGUAGE: Japanese
FAMILY ACC. NUM. COUNT: 3
PATENT INFORMATION:

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
JP 62123348	A2	19870604	JP 1985-263016	19851122
JP 06079009	B4	19941005		
EP 192488	B1	19911016	EP 1986-301229	19860220
R: DE, GB, IT, NL				

PRIORITY APPLN. INFO.:

JP 1985-33101	A	19850220
JP 1985-143790	A	19850629

JP 1985-263016 A 19851122

AB The title chemical sensor is comprised of (1) 2-semiconductor layers bonded with an insulator interlayer, (2) source and drain regions formed sep. in the entire depth of the 1st semiconductor layer, (3) grooves formed in the 2nd semiconductor layer to the depth such that the source, drain and channel regions are exposed, (4) gate insulator layer formed in the groove over the source, drain and channel regions, (5) passivating insulator layers formed on both surfaces of the semiconductor laminate and on the inside wall of the grooves, and (6) electrodes connected to the source and drain regions via through holes formed in the passivation layer on the 1st semiconductor layer. A desired ion-selective membrane may be placed on the gate insulators. The field-effect transistor-type chemical sensors can be fabricated easily by using the so-called planar process, and exhibit excellent service life.

L11 ANSWER 10 OF 11 CAPLUS COPYRIGHT 2006 ACS on STN
ACCESSION NUMBER: 1986:489609 CAPLUS
DOCUMENT NUMBER: 105:89609
TITLE: Semiconductor devices
INVENTOR(S): Konuma, Takeshi; Sugawa, Toshio
PATENT ASSIGNEE(S): Matsushita Electric Industrial Co., Ltd., Japan
SOURCE: Jpn. Tokkyo Koho, 4 pp.
CODEN: JAXXAD
DOCUMENT TYPE: Patent
LANGUAGE: Japanese
FAMILY ACC. NUM. COUNT: 1
PATENT INFORMATION:

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
JP 61004200	B4	19860207	JP 1978-71703	19780613
JP 54162461	A2	19791224		

PRIORITY APPLN. INFO.: JP 1978-71703 A 19780613

AB The semiconductor device is prepared by depositing 3 insulating layers on a semiconductor substrate and forming holes on these insulators. Part of the first insulating layer is exposed, and high dopant concentration regions are formed by ion injection. Parts of 1st and 3rd insulating layers are removed and metal electrodes are attached. For example, GaAs substrate and GaAs semiconductor layers were covered with SiO2 and Si3N4 insulators. Source and drain electrodes are then formed on the n+ region. The method was used to prepare field-effect transistors.

L11 ANSWER 11 OF 11 INSPEC (C) 2006 IET on STN
ACCESSION NUMBER: 1984:2190099 INSPEC
DOCUMENT NUMBER: B1984-009700
TITLE: Contact hole formation in integrated circuits using ion beam nitriding
AUTHOR: Bhagat, J.K.; Troxell, J.R. (Electronics Dept., General Motors Res. Labs., Warren, MI, USA)
SOURCE: Journal of the Electrochemical Society (Nov. 1983), vol.130, no.11, p. 2293-5, 6 refs.
CODEN: JESOAN, ISSN: 0013-4651
DOCUMENT TYPE: Journal
TREATMENT CODE: Practical
COUNTRY: United States
LANGUAGE: English
AN 1984:2190099 INSPEC DN B1984-009700
AB A method of opening contact holes through phosphosilicate glass (PSG) and thermally grown silicon dioxide to the underlying diffused source-drain regions and diffused polysilicon gates of MOSFETs (metal oxide semiconductor

field effect transistor) which minimizes the problem of contact blooming and resultant gate to source or drain shorts is described. In the fabrication of MOSFET integrated circuits, making contact holes to the source, drain, and gate is the last step prior to metallization. Improper contact holes can cause either an open circuit or a short circuit between adjacent circuit elements in an otherwise properly processed device or circuit. Due to this fact, contact holes are opened carefully and elaborate processing techniques are used in the industry. The authors have found that the presently available techniques are neither simple nor completely reliable. In this note, an alternative technique for opening the contact holes is presented

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